

FIG. 1
(PRIOR ART)

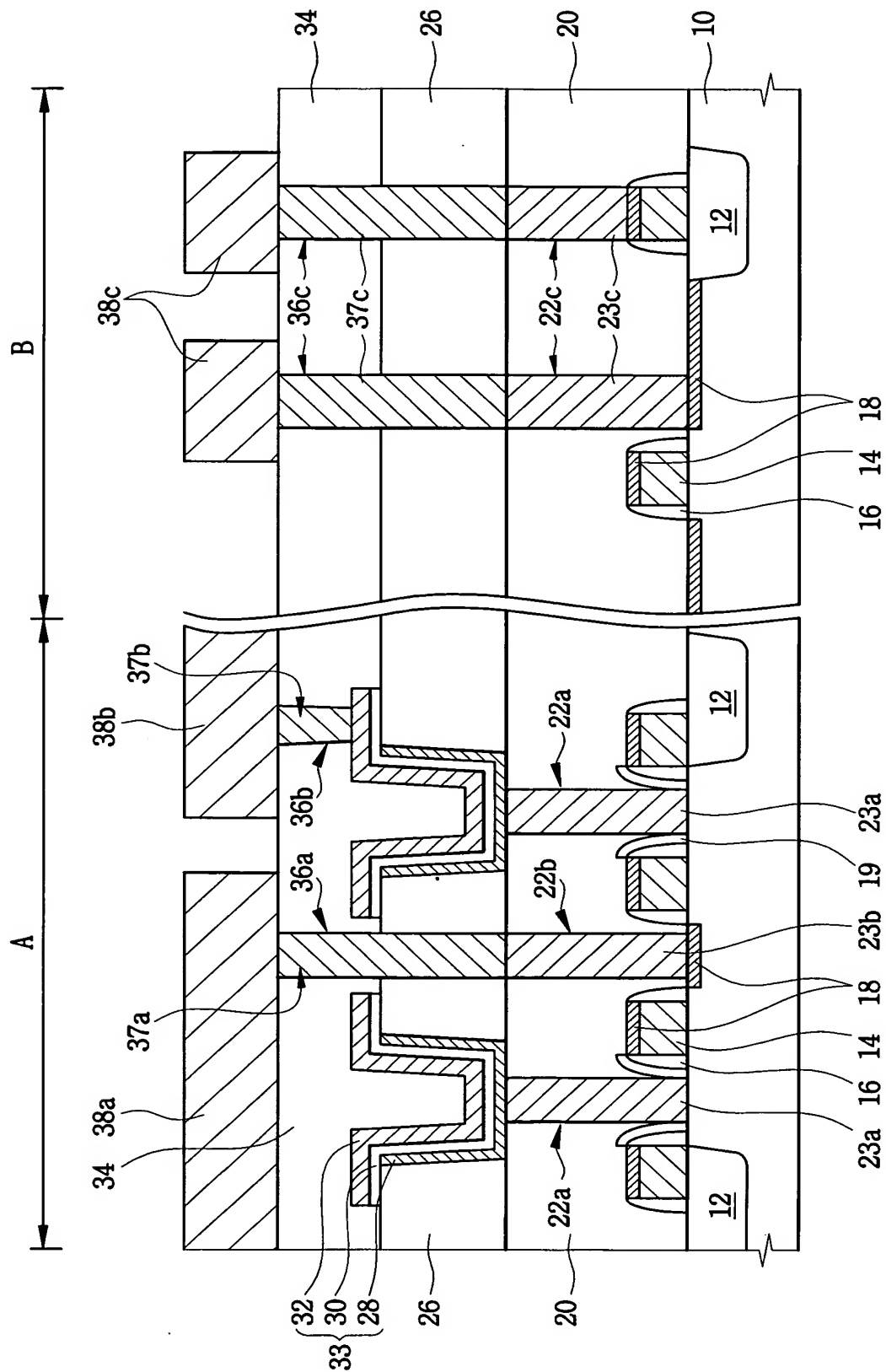


FIG. 2

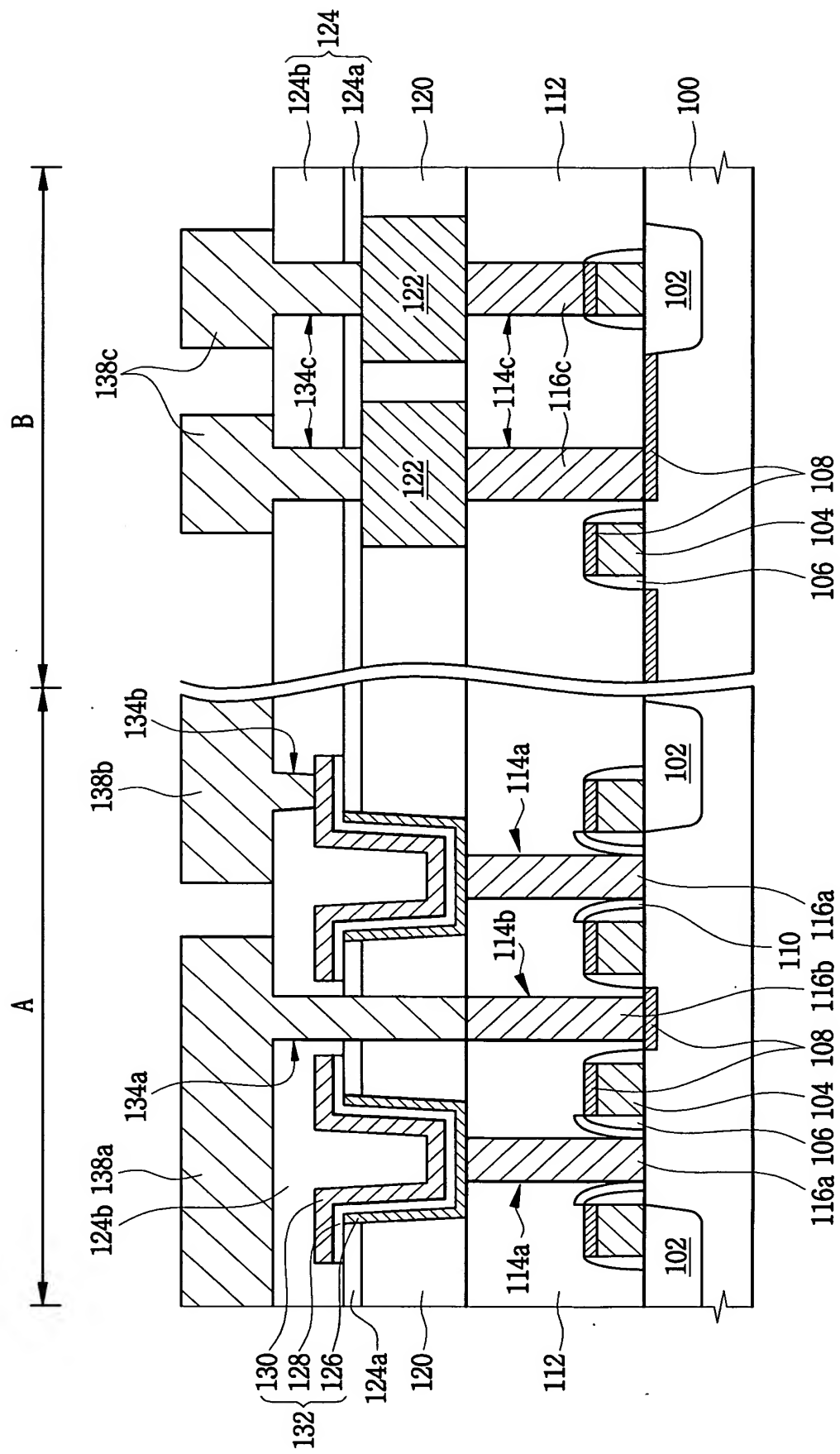


FIG. 3A

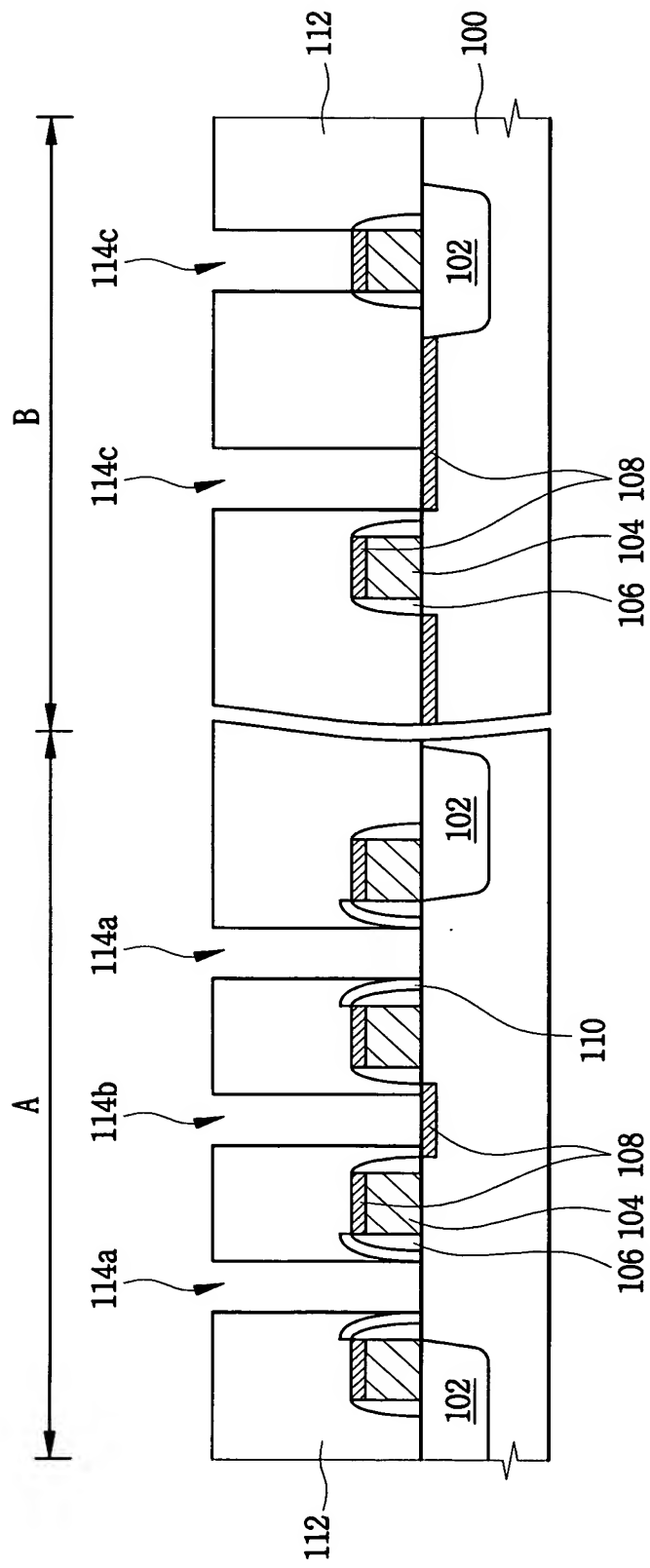


FIG. 3B

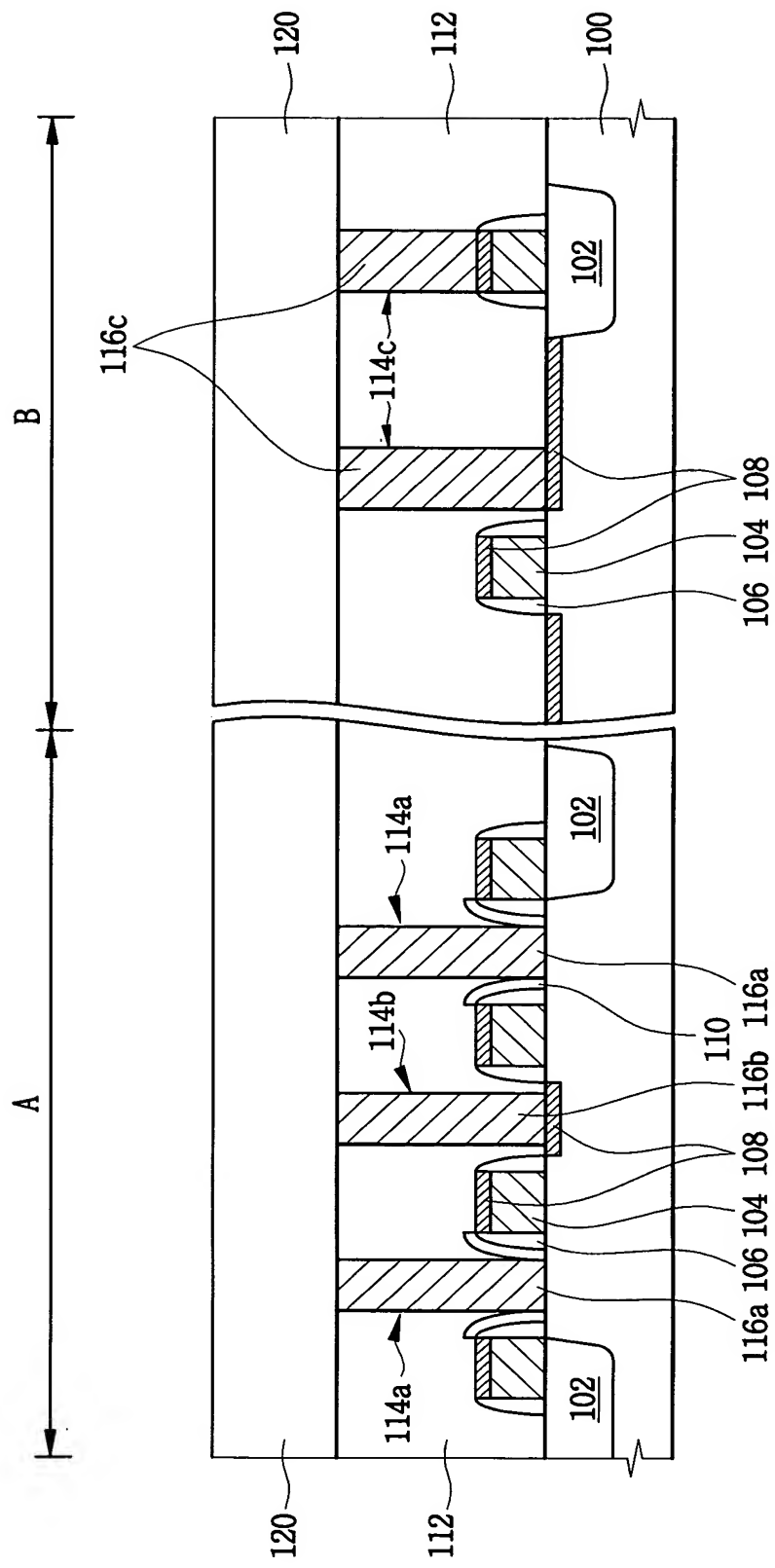


FIG. 3C

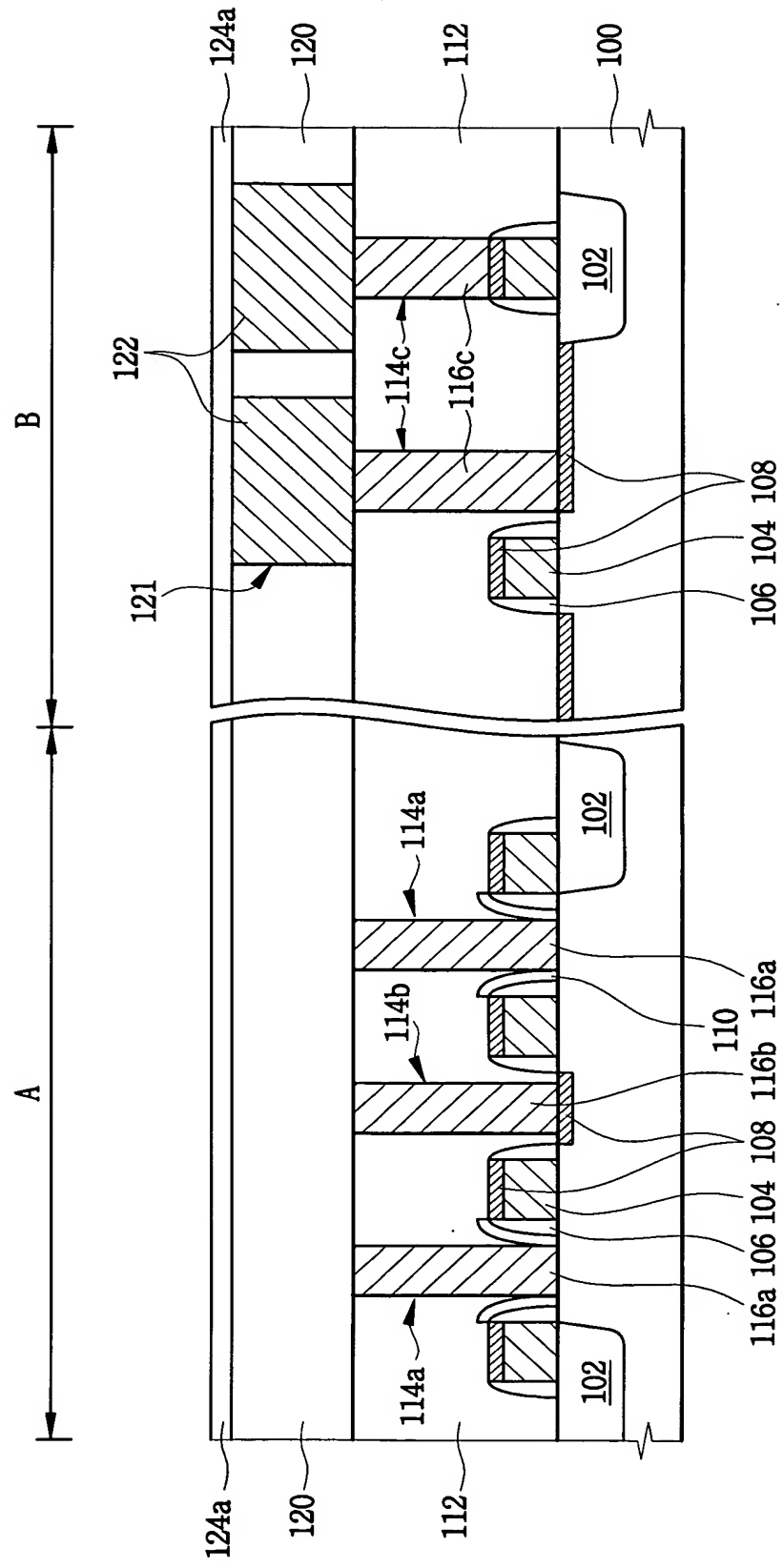


FIG. 1 is a cross-sectional view of a semiconductor device 100. The device includes a substrate 110 with a top surface 102. A gate stack 112 is formed on the substrate, comprising gate electrodes 114a, 114b, and 114c. A source/drain region 120 is formed on the substrate, with a source/drain electrode 124a. A contact layer 122 is formed on the source/drain region. A passivation layer 125 is formed on the top surface of the device. Dimensions A and B are indicated.

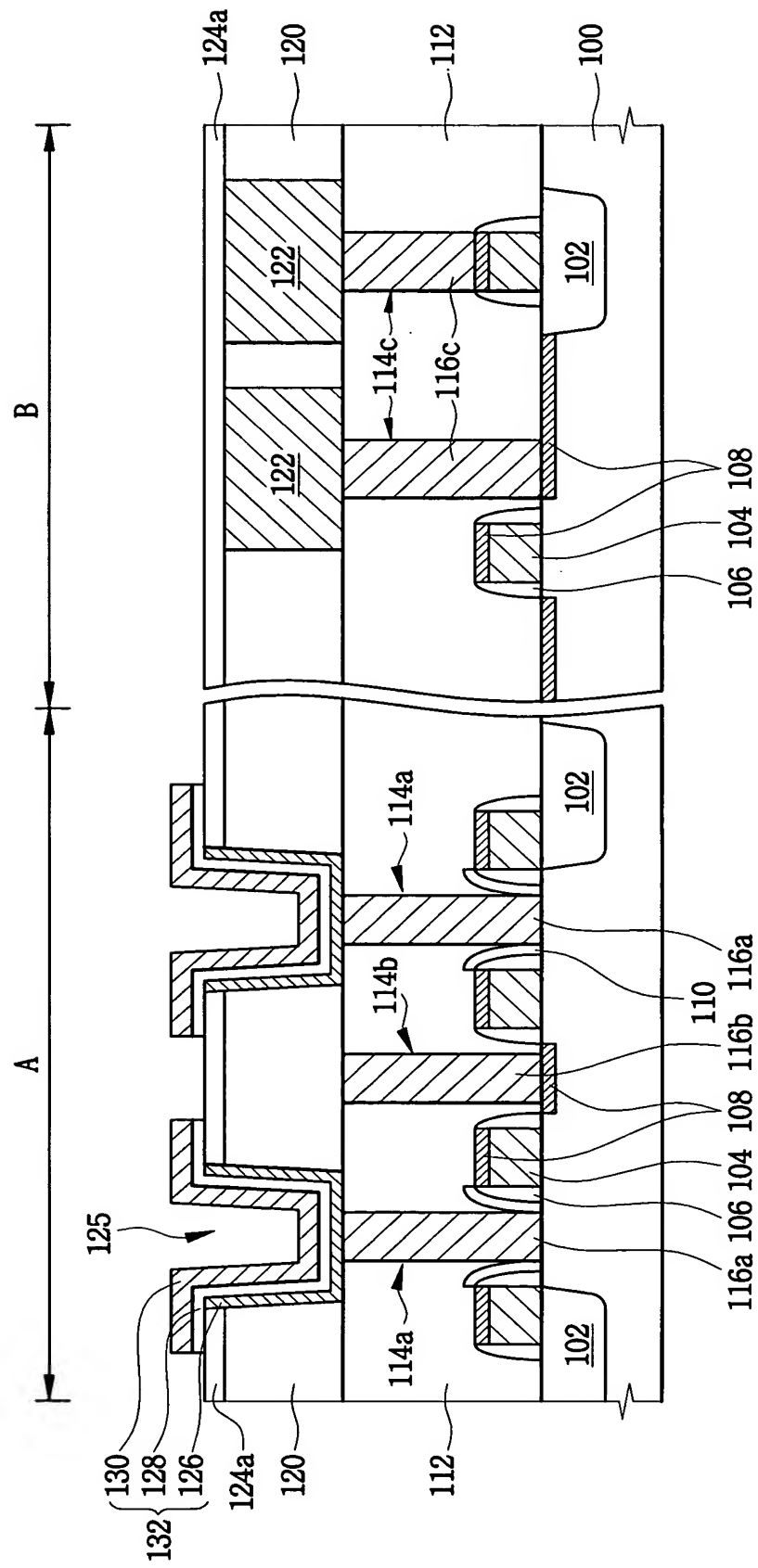
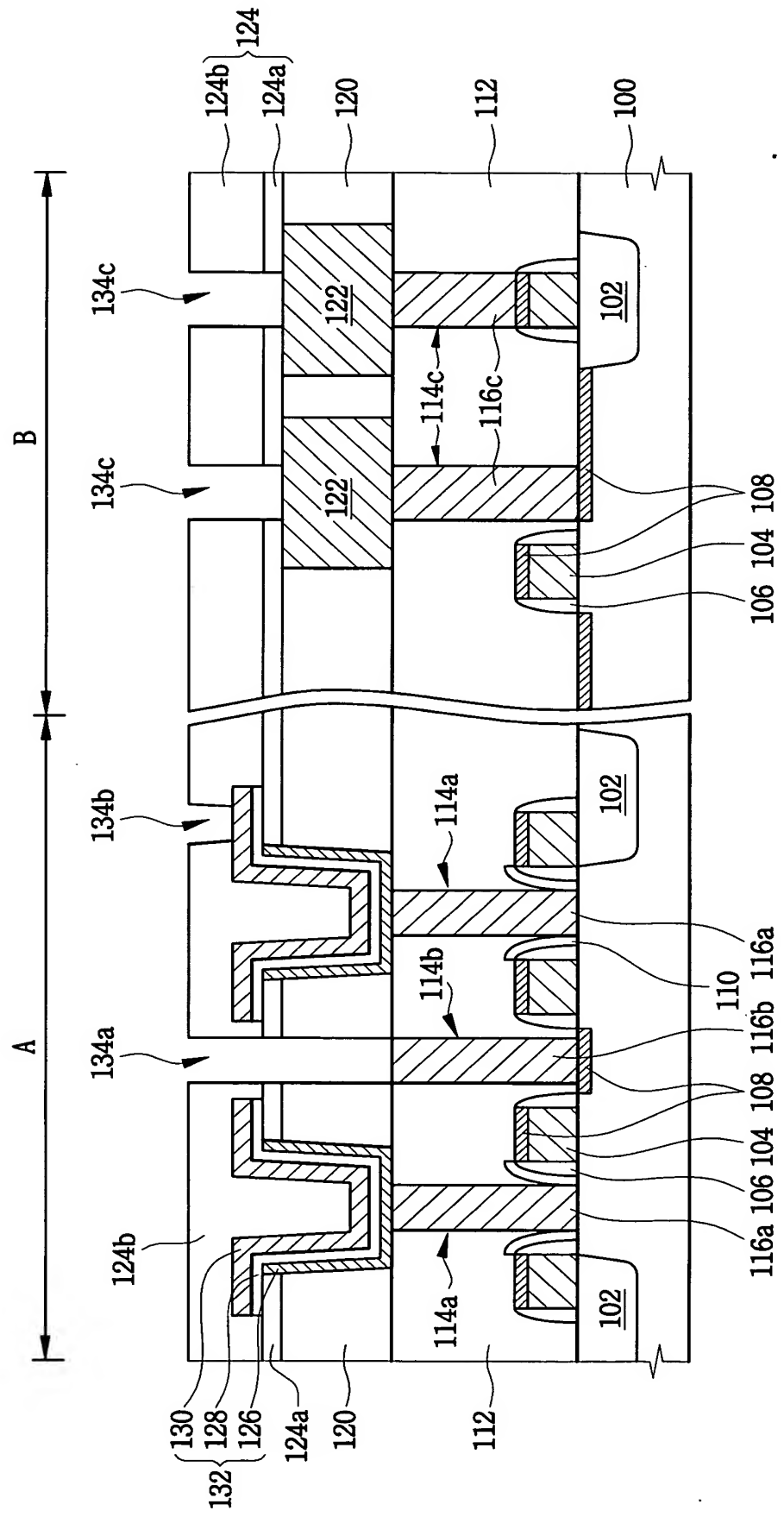


FIG. 3E



[illegible]

116a 106 104 108 116b 116a

FIG. 4A

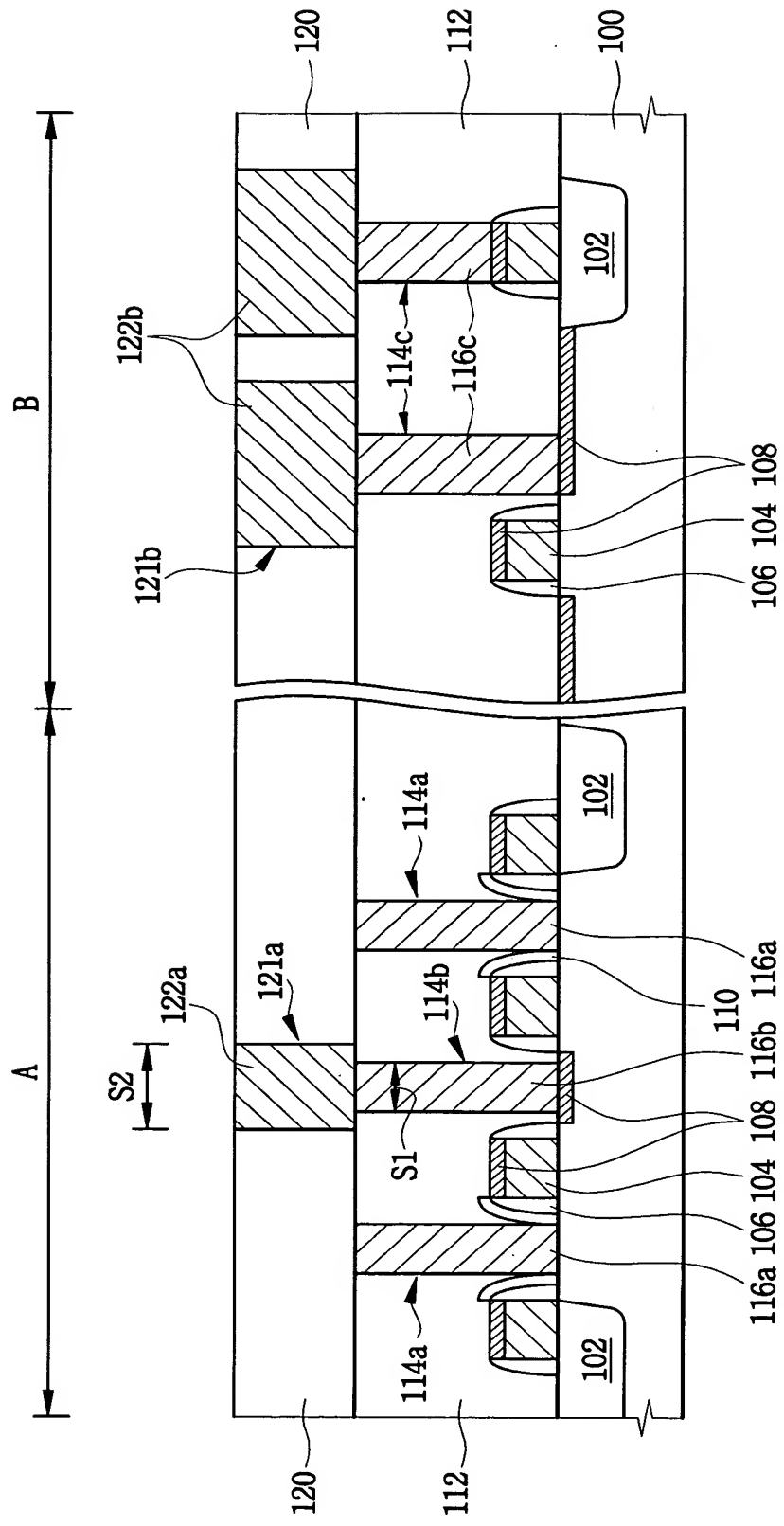


FIG. 4B

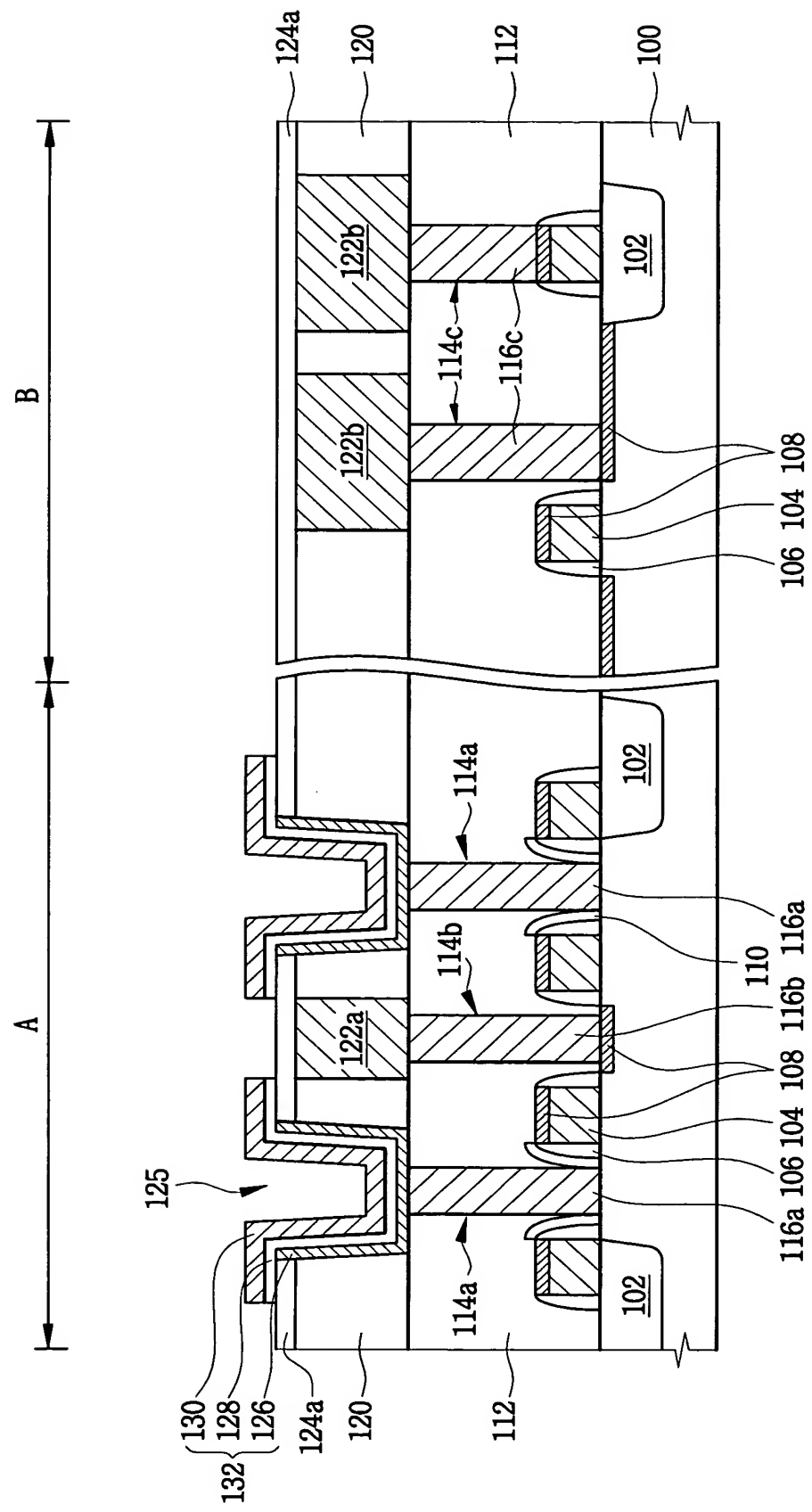


FIG. 4C

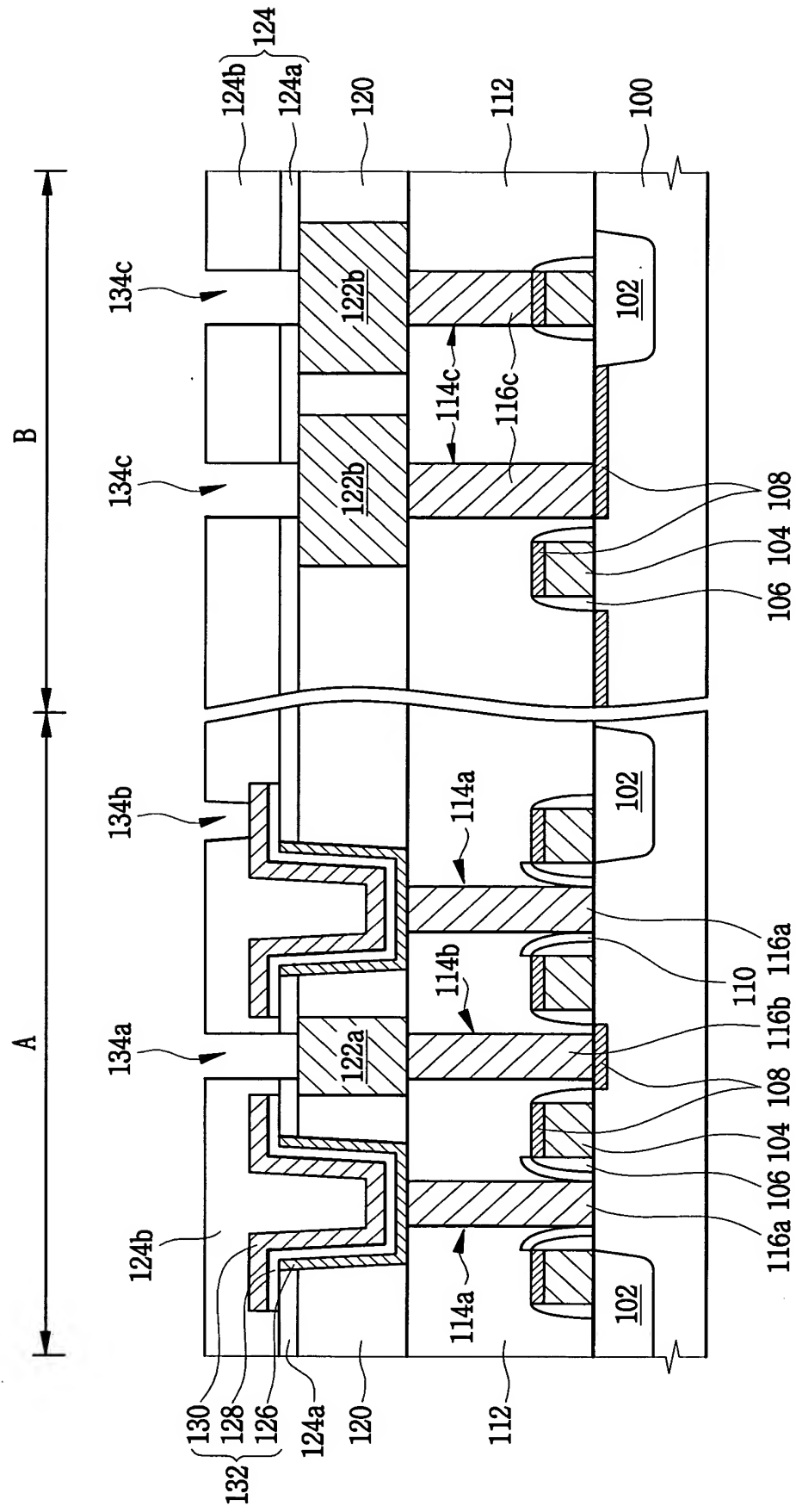


FIG. 1 is a cross-sectional view of a semiconductor device 100. The device includes a substrate 102 with a top layer 110. A series of gate structures 112 are formed on the substrate, each comprising a gate dielectric 114a, 114b, 114c and a gate electrode 116a, 116b, 116c. A conductive layer 120 is deposited over the gate structures. A patterned conductive layer 124a, 124b, 124c is formed on top of the conductive layer 120. A series of contact structures 130, 132, 134a, 134b, 134c are formed in the conductive layer 120, each comprising a contact dielectric 138a, 138b, 138c and a contact electrode 126a, 126b, 126c. The device is divided into two regions A and B by a vertical line 122a, 122b, 122c.

106 104 108